REMARKS/ARGUMENTS

Claims 25-33 are active in the present application, and have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakano (JP 6-291202) in view of Okumura (U.S. Patent No. 4,984,055). Applicant respectfully traverses the rejection.

The Examiner asserts that Nakano teaches a semiconductor device having a substrate, an insulating film (12) on the substrate, wirings (13) on insulating film (12), and a passivation layer covering a surface of the insulating film and wirings. The Examiner then cites to Okumura to show an interlayer insulating film and wirings located on the interlayer insulating film. The Examiner concludes that it would be obvious to combine the Nakano and Okumura et al. to provide the claimed invention.

It is well established that, in order to have *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference(s) must teach or suggest all of the claim limitations. MPEP § 2142.

Applicant submits that the Examiner has not established *prima facie* obviousness of the claimed invention. Specifically, the references do not teach or suggest all of the claim limitations, and there is no suggestion or motivation to modify the references in the way the Examiner suggests. Independent claims 25 and 31 require, among other things, "a passivation film covering *top surfaces* of the interlayer insulating film and the wirings" (emphasis added). Furthermore, independent claims 25 and 31 require that "no wiring is present on the passivation film." There is no teaching or suggestion provided in Nakano nor Okumura for a semiconductor device which includes which includes passivation film as claimed. In fact, Applicant submits that, if anything, the cited references teach away from using the structures of Nakano and Okumura as a passivation film covering top surfaces of the interlayer insulating film and wirings.

As noted in the English language abstract accompanying the Nakano reference, "the semiconductor substrate does not react with moisture in atmosphere which does not generate swelling effect in the SOG films *before forming a layer to layer insulation film.*" (Emphasis added). This description indicates that the structure of Nakano, similar to the structure of

Okumura, is specifically required to be an interlayer insulation film. The SOG films used in each of these references is utilized to planarize the surface of the semiconductor device, and not used to protect the wirings. As is well known, swelling in a SOG layer having contact or via holes may cause problems with a semiconductor device.

The Examiner argues that language within Nakano states that a wiring is not required to be formed on top of the SOG film. Applicant respectfully requests that the Examiner specifically point out this language from Nakano, such as by paragraph number or a copy of the reference which is marked to show the language. Applicants submit, to the contrary, that Nakano is specifically directed to an interlayer insulation film having a SOG film which is resistant to swelling if left in the atmosphere prior to deposition of a layer to layer insulation film. As indicated in the English language abstract (copy attached), the purpose of the device of Nakano is "to manufacture a semiconductor device excellent in *stepped part covering property and reliability of a multilayer interconnection* without lowering the flatness of an inorganic insulating film formed by application and firing of a solution" (emphasis added). Furthermore, Applicant submits that support indicating this reference is specifically directed to interlayer insulating films comes from the importance of a planarized film as described in the reference. This is evident from the language "without lowering the flatness" contained in the abstract. As is well known in the art, planarization is of high importance for interlayer insulating films in devices having multilayer metallization. However, planarization of the top passivation film is not as important, since no additional device layers will be deposited on the top layer. Nakano is thus specifically directed to an interlayer insulation film. Thus, Applicant submits that this reference does not teach or suggest a passivation film as claimed.

Furthermore, Applicant submits that none of the cited references, alone or in combination, teach or suggest a semiconductor device in which "no wiring is present on the passivation film," as required by independent claims 25 and 31. To the contrary, Nakano teaches in the specification, forming an Al wiring arranged on an interlayer insulating film on a second SOG film (16). Applicants submit, similarly as described above, that this description teaches away from using the second SOG film (16) as a passivation film as claimed. Okumura discloses a polysilicon layer (16) arranged on an oxide layer (14) on an intermediate SOG layer (13), as illustrated in Fig. 13D, for example. Accordingly, the SOG layer (16) does not function as a

passivation film as claimed. Accordingly, Applicant submits that the invention, as claimed in claims 25 and 31, is not obvious over the combination of Okumura and Nakano, and that claims 25 and 31 are allowable over the cited references. Furthermore, Applicant submits that Claims 26-30, and 32-33, which depend (directly or indirectly) from the independent claims, are also allowable over the cited references for at least the same reasons as described with respect to the independent claims.

The Examiner also states that the claimed limitation of "no wiring is present on the passivation film" means that Applicant claims an intermediate product, because the claimed device would not operate if external wiring are not connected thereto. Applicant respectfully disagrees with the Examiner. The claim preamble in each independent claim 25 and 31 recites "A semiconductor device...." The semiconductor device, as claimed, is not an intermediate product, but rather a complete semiconductor device. External bonding wires, as are well known in the art, are one method of connecting such devices to external devices through bonding pad regions which are present in the passivation film. Accordingly, as claimed, the semiconductor device is a complete device which may be connected to external circuitry through, for example, external bonding wires.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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